Hao Yu

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Education

2014–present **PhD, Computer Science**, *University of California, Los Angeles*, Los Angeles, CA.
Advisor: Professor Jason Cong
2011–2013 **MS, Computer Science**, *National Tsing Hua University*, Hsinchu, Taiwan.
Advisor: Professor Shih-Chieh Chang
Thesis: Package-Aware Thermal Analysis and Reliable 3DIC Design
2007–2011 **BS, Computer Science**, *National Tsing Hua University*, Hsinchu, Taiwan.
GPA: 3.65/4.0 (CS major: 3.9/4.0)

Research Experience

University of California, Los Angeles

2015–present **Big Data Analysis on Heterogeneous Platforms** .
The explosion of the scale and complexity in modern applications are impractical to be executed by single thread. As a result, cloud computing technology is presented to solve this problem by using not only multi-thread but multiple machines. The followed problem of power and energy have been risen. Adapting heterogeneous devices such as FPGA as accelerators for certain application domains is one of the best solution. However, FPGA is difficult to be included because of its poor programmability. In this project, we attempt to develop a framework that allows programmers to program their MapReduce applications in Java or Scala, and then translates a part of the application to OpenCL kernel to be accelerated by FPGAs.

2014–present **Impact on Loop Transformations of Software Reliability**.
Transient hardware faults induced soft-errors cannot be ignored due to technology scaling. Researchers in hardware field attempt to solve this problem by developing novel circuits and architectures. However, the additional hardware overhead is inevitable. In this project, we improve software reliability by analyzing the impact of loop transformations. We attempt to present a systematic metric to analyze the reliability impact of loop transformations, and further improve software reliability through suitable transformations.

National Tsing Hua University

2012–2013 **Package-Chip Thermal Co-Analysis**.
2011–2013 **Reliability-Aware Stacking Integrated Circuit Design**.
2010–2011 **Useful Clock Skew Optimization**.

Working Experience

2008–2009 **Part-Time Software Engineer**, *Taiwan Semiconductor Manufacturing Company Limited, tsmc*, Hsinchu, Taiwan.
Software development in FMCS, FAB12. Developed applications to help internal people monitoring facilities.

Honors

Mar. 2014 UCLA Computer Science Departmental Fellowship, UCLA.
Mar. 2014 UCLA Graduate Dean's Scholar Award (GDSA), UCLA.

Nov. 2012 Novatek Education Foundation Scholarship, Taiwan.

Nov. 2011 Novatek Education Foundation Scholarship, Taiwan.

June 2011 2nd place, 2011 CAD contest, Taiwan.

Apr. 2011 2nd place, TAU Power Grid Simulation Contest, CA.

Sept. 2011 NTHU Computer Science Double Degree Scholarship.

Oct. 2010 NTHU EECS Outstanding Student Scholarship, Taiwan.

Skills

Programming Languages *C/C++, Perl, Python, Java, Matlab, Verilog*

Software Infrastructure *LLVM, Aparapi, Spark*

VLSI Design Tools *DesignCompiler, HSpice, SoCE*

Teaching Experience

2013 **CS5100, Advanced Computer Architecture**, *NTHU, Taiwan.*.

Instructor: Associate Professor Hsien-Hsin S. Lee, Georgia Tech, Atlanta, GA.

2011, 2012 **CS3120, Introduction of Integrated Circuit Design**, *NTHU, Taiwan.*.

Instructor: Professor Shih-Chieh Chang, NTHU, Taiwan.

2012 **CS2104, Hardware Lab**, *NTHU, Taiwan.*.

Instructor: Professor Shih-Chieh Chang, NTHU, Taiwan.

Publications

Journal Publications

2014 Cody H. Yu, C.-L. Lung, Y.-L. Ho, R.-S. Hsu, K.-M. Kwai, and S.-C. Chang, "Thermal-Aware On-Line Scheduler for 3D Many-Core Processor Throughput Optimization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 33, Issue 5, pp. 763-773, May. 2014.

Conference Publications

2014 J.-H. Chien, H. Yu, R.-S. Hsu, H.-J. Lin and S.-C. Chang, "Package Geometric Aware Thermal Analysis by Infrared-Radiation Thermal Images," *Design, Automation & Test in Europe (DATE)*, 2014, No. 45.

2013 J.-H. Chien, H. Yu, C.-L. Lung, Y.-F. Chou, D.-M. Kwai, and S.-C. Chang, "IC-Package Co-design by Computational Thermographics," *in Proc. of International Microsystems, Package, Assembly Conference Taiwan (IMPACT)*, 2013. **(Nominated for Best Paper Award)**

2013 C.-H. Chou, N.-Y. Tsai, H. Yu, J.-H. Chien, Y. Shi and S.-C. Chang, "On the Futility of Thermal Through-Silicon-Vias," *in Proc. of International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, 2013.

2012 J.-H. Chien, H. Yu, C.-L. Lung, N.-Y. Tsai, H.-C. Chang, Y.-F. Chou, P.-H. Chen, S.-C. Chang and D.-M. Kwai, "Thermal Stress Aware Design for Stacking IC with Through Glass Via," *in Proc. of International Microsystems, Package, Assembly Conference Taiwan (IMPACT)*, 2012, pp. 133-136. **(Nominated for Best Paper Award)**

2012 J.-H. Chien, H. Yu, N.-Y. Tsai, C.-L. Lung, C.-C. Hsu, Y.-F. Chou, P.-H. Chen, S.-C. Chang and D.-M. Kwai, "Hybrid Thermal Solution for 3D-ICs: Using Thermal TSVs with Placement Algorithm for Stress Relieving Structures," *in Proc. of Electronic Components and Technology Conference (ECTC)*, 2012, pp. 1455-1460.

2011 C.-H. Chou, N.-Y. Tsai, H. Yu, C.-R. Lee, Y. Shi and S.-C. Chang, "On the Preconditioner of Conjugate Gradient Method: A Circuit Perspective," *in Proc. of International Conference on Computer Aided Design (ICCAD)*, 2011, pp. 494-497. **(Invited)**

2011 H.-M. Chou, H. Yu and S.-C. Chang, "Useful-Skew Clock Optimization for Multi-Power Mode Designs," *in Proc. of International Conference on Computer Aided Design (ICCAD)*, 2011, pp. 647-650.

Patents

2012 N.-Y. Tsai, H. Yu, J.-H. Chien and S.-C. Chang, "STRUCTURE AND MANUFACTURING METHOD FOR REDUCING STRESS OF CHIP," *pending to US patent, 13/535,083*, Jun. 27, 2012.

Master's Thesis

2013 H. Yu, "Package-Aware Thermal Analysis and Reliable 3DIC Design," Master's thesis, Computer Science Department, National Tsing Hua University, 2013.